

REMARKS

In the Official Action mailed on **9 August 2007**, the Examiner reviewed claims 1-45. Claims 1-8, 12-20, 23-30, 34-38, and 42-45 were rejected under 35 U.S.C. § 103(a) based on Brian et al. (US Pub. No. 2005/0129039 hereinafter “Brian”), and Payson (USPN 7,194,661 hereinafter “Payson”). Claims 9-11, 21-22, 31-33, and 39-41 were rejected under 35 U.S.C. § 103(a) based on Brian, Payson, and Boyd et al. (US Pub. No. 2006/0259644 hereinafter “Boyd”).

Rejections under 35 U.S.C. § 103(a)

Claims 1-8, 12-20, 23-30, 34-38, and 42-45 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Brian in view of Payson. Claims 9-11, 21-22, 31-33, and 39-41 were rejected under 35 U.S.C. § 103(a) as unpatentable over Brian in view of Payson, further in view of Boyd. Applicant respectfully disagrees because Brian, Payson, and Boyd fail to teach sharing a single contiguous memory with multiple queue pairs and virtual lanes.

Brian discloses performing direct data placement (DDP) to memory where all received DDP segments of a particular connection are aligned (see [0030] of Brian). In the Brian system, buffers are included in **each data transfer unit**, which could be a data source or a data sink (see [0060] and Fig. 2A of Brian). In other words, the Brian system uses a dedicated queue for each data transfer unit. Therefore, Brian teaches away from sharing a single contiguous memory structure by assigning each queue pair a pair of work queues (eg., send and receive queues) (see [0020] of Brian). Note that dedicated queues require each queue pair and virtual lane to be provided with worst-case buffering, thus resulting in an inefficient use of memory space.

Payson discloses providing an online system monitoring technique to identify failures or other system errors (see col. 2, ll. 10-23 of Payson). In the

Payson system, input/output cards are used for transmitting and receiving packets on a **per virtual lane/queue** basis (see col. 5, 30-35, col. 6, 59-62, and col. 7, 22-24 of Payson). Similarly, Payson teaches away from sharing a single contiguous memory structure by assigning one output queue for each virtual lane (see Fig. 6 and col. 7, 34-47 of Payson).

Furthermore, Boyd discloses assigning **each queue pair** a send working queue and receive work queue (see [0071], [0085], Figs. 4-5 of Boyd) and **using multiple queues for multiple queue pairs** (see [0068] of Boyd). Hence, the Boyd system also does not teach sharing a single contiguous memory among queue pairs and virtual lanes.

In contrast, the embodiments of the present invention involve mapping outbound communications, and in a channel adapter or other interface devices, a single contiguous memory structure is shared among multiple queue pairs and virtual lanes (see page 4, ll. 13-26 of the instant application). There is nothing in Brian, Payson and Boyd, either explicit or implicit, that teaches sharing a single contiguous memory structure among multiple queue pairs and virtual lanes.

Accordingly, Applicant has amended claims 1, 13, 16, 29, 34, and 38 to clarify that the present invention shares a single contiguous memory structure among multiple queue pairs and virtual lanes. These amendments find support in page 13, ll. 1-6 of the instant application. No new matter has been added.

Hence, Applicant respectfully submits that independent claims 1, 13, 16, 29, 34 and 38 as presently amended are in condition for allowance. Applicant also submits that claims 2-12, which depend upon claim 1, claims 14-15, which depend upon claim 13, claims 17-28, which depends upon claim 16, claims 30-33, which depend upon claim 29, claims 35-37, which depend upon claim 34, and claims 39-45, which depend upon claim 38, are for the same reasons in condition for allowance and for reasons of the unique combinations recited in such claims.

